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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,778	03/06/2002	Robin Alexis Takasugi	10018457-1	8925

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EXAMINER	
CORRIELUS, JEAN M	

ART UNIT	PAPER NUMBER
2162	

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,778	TAKASUGI ET AL.	
	Examiner	Art Unit	
	Jean M Corrielus	2162	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on February 1, 2005, in which claims 1-24 are presented for further examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Siegel US Patent no.5, 261,072.

As to claim 1, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the

register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56).

As to claim 7, Siegel discloses the claimed "wherein the host device is a computer" (col.4, lines 37-50).

As to claim 8, Siegel discloses the claimed "wherein the storage medium comprises non-volatile semiconductor memory" (col.6, lines 15-62).

As to claim 9, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-6 and 10-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siegel US Patent no. 5,261,072 and Gharachorloo et al., (hereinafter "Gharachorloo") US Patent no. 6,748,498.

As to claims 2- 6 and 13-17, Siegel discloses the use of storing in the third register a value for incrementing a value contained in the first register" (col.7, lines 33-35); incrementing a value contained in the first register by the value contained in the register (col.7, lines 45-56); storing in the register an address representing a location in the buffer where data is being transferred between the buffer and the host device (col.8, lines 5-65): storing in the register an address representing a location in the buffer where data is being transferred between the buffer and storage medium (col.8, lines 5-65); storing in a sixth register an address representing a beginning of the buffer (col.8, lines 5-65); storing in the register an address representing and end of the buffer (col.8, lines 5-67) and storing in the register a value representing a storage capacity of the buffer (col.8, lines 5-65). However, Siegel does not explicitly disclose the use of second-eight registers. On the other hand, discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data (col.9, lines 19-27). In particular, has shown that the current state of multiple memory transactions is stored in a set of registers collectively called the transient state register, wherein each memory transaction has a respective entry stored in the transient state register that indicates the state of each memory transaction (col.13, lines 43-65; col.14, lines 1-8; col.15, lines 60-67). These implications disclose the use of a second-eight register, wherein each one of the registers performs their own task. It would have been obvious

to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 10, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out the buffer" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "modifying the value contained in the first register in response to a transfer of a data unit out of the buffer" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "modifying a value contained in the first register in response to a transfer of a data unit into the buffer" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second and third register. On the other hand, discloses an analogous system that provides the use of

determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data (col.9, lines 19-27). In particular, has shown that the current state of multiple memory transactions is stored in a set of registers collectively called the transient state register, wherein each memory transaction has a respective entry stored in the transient state register that indicates the state of each memory transaction (col.13, lines 43-65; col.14, lines 1-8; col.15, lines 60-67). These implications disclose the use of a second and third register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claim 11, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the host device" (col.7, lines 33-65; col.8, lines 5-67).

As to claim 12, Siegel discloses the claimed "wherein the data transfer system is configured to modify the value contained in the first register in response to a transfer of a data unit between the buffer and the storage medium" (col.7, lines 33-65).

As to claim 18, Siegel discloses the claimed "implementing the method via an application specific integrated circuit (ASIC) (col.4, lines 1-9; col.7, lines 50-66).

As to claims 19-21, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second and third register. On the other hand, discloses an analogous system that provides the use of determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data (col.9, lines 19-27). In particular, has shown that the current state of multiple memory transactions is stored in a set of registers collectively called the transient state register, wherein each memory transaction has a respective entry stored in the transient state register that indicates the state of each memory transaction (col.13, lines 43-65; col.14, lines 1-8;

col.15, lines 60-67). These implications disclose the use of a second and third register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

As to claims 22-24, Siegel discloses the claimed "receiving from the host device a command to transfer data between the host device and the storage medium" an implemented software used to execute a software call from a supervisory program operating in the host computer to receive the commands to transfer data to the storage medium (Abstract; col.3, lines 48-64); "temporarily stores data that is transferred between the host device and the storage medium" (col.3, lines 40-50); "storing in a first register a value for determining a buffer's fullness" (col.6, lines 58-67; since register in general used to hold data for a particular purpose so the memory cache as disclosed by Siegel has the register that allow to hold the amount of data to be transferred col.3, line 66-col.4, line 9) and "decrementing the value contained in the first register" by decrementing the value contained in the first register to zero which indicated that all the requested data has been transferred (col.7, lines 33-35) and "incrementing the value contained in the first register" by incrementing the value contained in the register in response to a transfer of a data into the buffer (col.7, lines 46-56). However, Siegel does not explicitly disclose the use of second and third register. On the other hand, discloses an analogous system that provides the use of

determining which data transfer(s) to handle during each available data transfer period, wherein the data transfers generally are sent with a command or transaction type indicator, which is transferred in parallel with the first bits of data (col.9, lines 19-27). In particular, has shown that the current state of multiple memory transactions is stored in a set of registers collectively called the transient state register, wherein each memory transaction has a respective entry stored in the transient state register that indicates the state of each memory transaction (col.13, lines 43-65; col.14, lines 1-8; col.15, lines 60-67). These implications disclose the use of a second and third register, wherein each one of the registers performs their own task. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of the cited references, wherein the host computer provided therein (see Siegel's fig.1 item 14) would incorporate the use of a multiple registers, wherein each one the register would perform their own specific task. One having ordinary skill in the art would have found it motivated to utilize such a combination in order to ensure integrity of the transfer.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean M Corrielus whose telephone number is (571) 272-4032. The examiner can normally be reached on 10 hours shift.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on (571) 272-4107. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean M Corrielus
Primary Examiner
Art Unit 2162

April 4, 2005